IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A microprocessor to which a plurality of memory units including a first memory unit and a second memory unit and having physical addresses different from each other are externally connected, said microprocessor comprising:

a first address conversion unit which carries out a first address conversion by assigning a first physical address of said first ~~said~~ memory unit to a first logical address of a load module stored in [[a]] said first memory unit, wherein said load module includes an instruction code and numerical data;

a copying unit which copies said instruction code from said load module stored in said first memory unit to said second memory unit ~~out of said plurality of memory units~~; and

a second address conversion unit which carries out a second address conversion different from the first address conversion by assigning a second physical address of said second memory unit to a second logical address of the instruction code copied to said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said first logical ~~addressed~~ address, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said second logical address.

2. (Original) The microprocessor according to claim 1, wherein when said load module stored in said second memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

3. (Original) The microprocessor according to claim 1, wherein said load module stored in said first memory unit includes data for image processing and the instruction codes for image processing.

4. (Currently Amended) A microprocessor to which a plurality of memory units including a first memory unit and a second memory unit and having physical addresses different from each other are externally connected, said microprocessor comprising:

a first address conversion unit which carries out a first address conversion by assigning a first physical address of said [[a]] first memory unit to a first logical address of a load module stored in [[a]] said first memory unit, wherein said load module includes an instruction code and numerical data;

a processing unit which temporarily stores and copies said instruction code from said load module stored in said first memory unit to said [[a]] second memory unit; and

a second address conversion unit which carries out a second address conversion different from the first address conversion by assigning a second physical address of said second memory unit to a second logical address of the instruction code copied to said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said first logical address, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said second logical address.

5. (Original) The microprocessor according to claim 4, wherein when said load module stored in said second memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

6. (Original) The microprocessor according to claim 4, wherein said load module stored in said first memory unit includes data for image processing and the instruction codes for image processing.

7. (Currently Amended) A ~~memory~~ device comprising:

a plurality of memory units including a first memory unit ~~including a first memory unit~~ and a second memory unit and having physical addresses different from each other;

a first address conversion unit which carries out a first address conversion by assigning a first physical address of said [[a]] first memory unit to a first logical address of a load module stored in said first memory unit, wherein said load module includes an instruction code and numerical data;

a copying unit which copies said instruction code ~~from said and instruction code~~ from said load module stored in said first memory unit to said second memory unit; and

a second address conversion unit which carries out a second address conversion different from the first address conversion by assigning a second physical address of ~~said second physical address of~~ said second memory unit to a second logical address of the instruction code copied to said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said first logical address, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said second logical address.

8. (Currently Amended) The ~~memory~~ device according to claim 7, wherein when said load module stored in said second memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

9. (Currently Amended) The ~~memory~~ device according to claim 7, wherein said load module stored in said first memory unit includes data for image processing and the instruction codes for image processing.

10. (Currently Amended) The ~~memory~~ device according to claim 7, wherein the access speed of said second memory unit is faster than the access speed of said first memory unit.

11. (Currently Amended) The ~~memory~~ device according to claim 10, wherein said second memory unit ~~is constituted of~~ comprises a synchronous DRAM.

12. (Currently Amended) A ~~memory~~ device comprising:

a plurality of memory units including a first memory unit and a second memory unit and having physical addresses different from each other;

a first address conversion unit which carries out a first address conversion by assigning a first physical address of said [[a]] first memory unit ~~out of said plurality of memory units~~ to a first logical address of a load module stored in said first memory unit, wherein said load module includes an instruction code and numerical data;

a processing unit which temporarily stores and copies said instruction code from said load module stored in said first memory unit to said second memory unit; and

a second address conversion unit which carries out a second address conversion different from the first address conversion by assigning a second physical address of said second memory unit to a second logical address of the instruction code copied to said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said first logical address ~~assigned with said physical address of said first memory unit~~, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said second logical address.

13. (Currently Amended) The ~~memory~~ device according to claim 12, wherein when said load module stored in said first memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

14. (Currently Amended) The ~~memory~~ device according to claim 12, wherein said load module stored in said first memory unit includes data for image processing and ~~the instruction codes for~~ image processing instruction codes.

15. (Currently Amended) The ~~memory~~ device according to claim 12, wherein the access speed of said second memory unit is faster than the access speed of said first memory unit.

16. (Currently Amended) The ~~memory~~ device according to claim 15, wherein said second memory unit ~~is constituted of~~ comprises a synchronous DRAM.

17. (Previously Presented) The microprocessor of claim 1, wherein the operating speed of the second memory unit is faster than the operating speed of the first memory unit.

18. (Canceled)

19. (Previously Presented) The microprocessor according to claim 1, wherein the first address conversion unit carries out the first address conversion for information including the numerical data.

20. (Previously Presented) The microprocessor according to claim 1, wherein the second address conversion unit carries out the second address conversion for the instruction code.

21. (Previously Presented) The microprocessor according to claim 4, wherein the first address conversion unit carries out the first address conversion for information including the numerical data.

22. (Previously Presented) The microprocessor according to claim 4, wherein the second address conversion unit carries out the second address conversion for the instruction code.

23. (Currently Amended) The ~~memory~~ device according to claim 7, wherein the first address conversion unit carries out the first address conversion for information including the numerical data.

24. (Currently Amended) The ~~memory~~ device according to claim 7, wherein the second address conversion unit carries out the second address conversion for the instruction code.

25. (Currently Amended) The ~~memory~~ device according to claim 12, wherein the first address conversion unit carries out the first address conversion for information including the numerical data.

26. (Currently Amended) The ~~memory~~ device according to claim 12, wherein the second address conversion unit carries out the second address conversion for the instruction code.

27. (New) A method of accessing a plurality of memory units, including a first memory unit and a second memory unit, the memory units having differing physical addresses, the method comprising:

a first address conversion step which carries out a first address conversion by comparing a requested logical address with a first logical address and assigning a first physical address of said first memory unit to a load module logical address for a load module stored in said first memory unit, wherein said load module includes an instruction code and numerical data;

a copying step which copies said instruction code from said load module stored in said first memory unit to said second memory unit; and

a second address conversion step which carries out a second address conversion different from the first address conversion by comparing said requested logical address with a second logical address and assigning a second physical address of said second memory unit to an instruction code logical address for the instruction code copied to said second memory unit.

28. (New) The method according to claim 27, wherein when said load module stored in said second memory unit is accessed, the first address conversion step assigns the physical address of said first memory unit to the load module logical address of said load module to be accessed, and the second address conversion step assigns the physical address of said second memory unit to said instruction code logical address of the instruction code from said load module to be accessed.

29. (New) The method according to claim 27, wherein said load module stored in said first memory unit includes data for image processing and image processing instruction codes.

30. (New) The method according to claim 27, wherein the first address conversion step carries out the first address conversion for information including the numerical data.

31. (New) The method according to claim 27, wherein the second address conversion step carries out the second address conversion for the instruction code.

32. (New) A method of accessing a plurality of memory units, the memory units including a first memory unit and a second memory unit, wherein the memory units have differing physical addresses, the method comprising:

a first address conversion step which carries out a first address conversion by comparing a requested logical address with a first logical address and assigning a first physical address of said first memory unit to a load module logical address of a load module stored in said first memory unit, wherein said load module includes an instruction code and numerical data;

a processing step which temporarily stores and copies said instruction code from said load module stored in said first memory unit to said second memory unit; and

a second address conversion step which carries out a second address conversion different from the first address conversion by comparing said requested logical address with a second logical address and assigning a second physical address of said second memory unit to an instruction code logical address of the instruction code copied to said second memory unit.

33. (New) The method according to claim 32, wherein when said load module stored in said second memory unit is accessed, the first address conversion step assigns the physical address of said first memory unit to the load module logical address of said load module to be accessed, and the second address conversion step assigns the physical address of said second memory unit to said instruction code logical address of the instruction code from said load module to be accessed.

34. (New) The method according to claim 32, wherein said load module stored in said first memory unit includes data for image processing and image processing instruction codes.

35. (New) The method according to claim 32, wherein the first address conversion step carries out the first address conversion for information including the numerical data.

36. (New) The method according to claim 32, wherein the second address conversion step carries out the second address conversion for the instruction code.